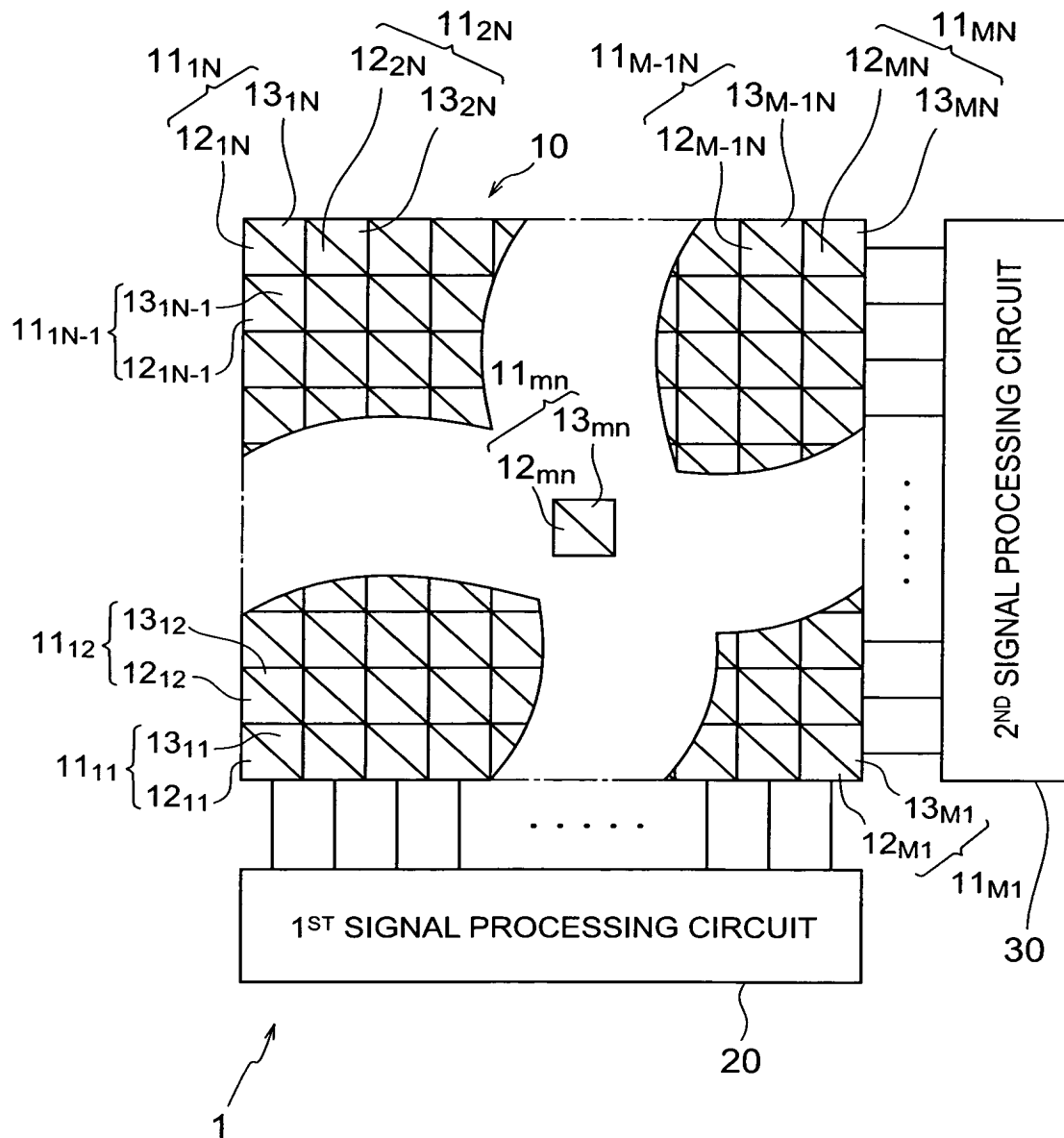
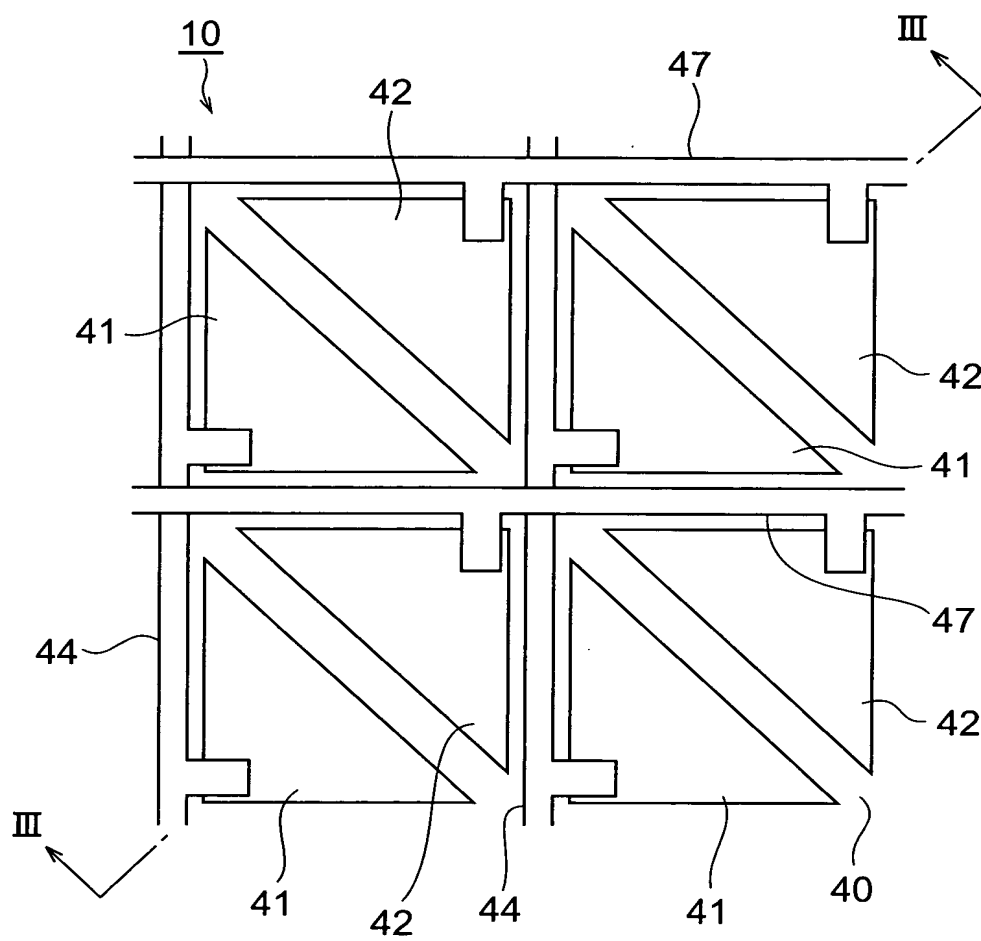
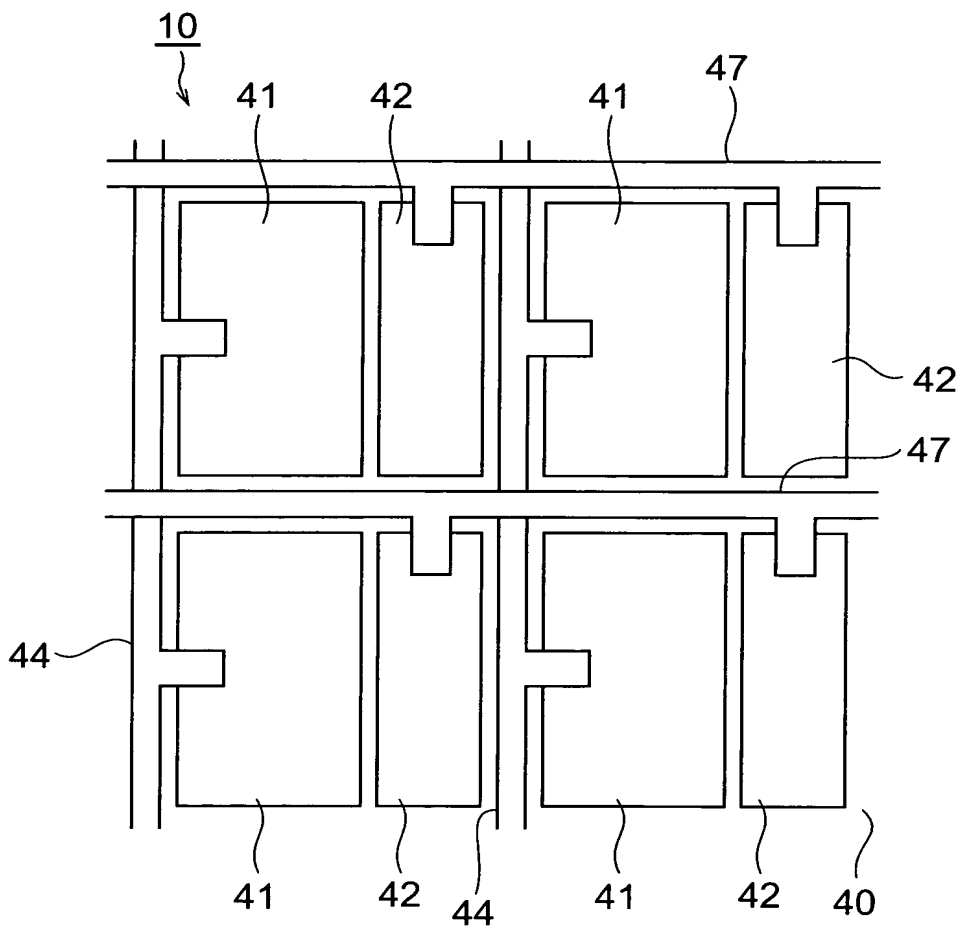


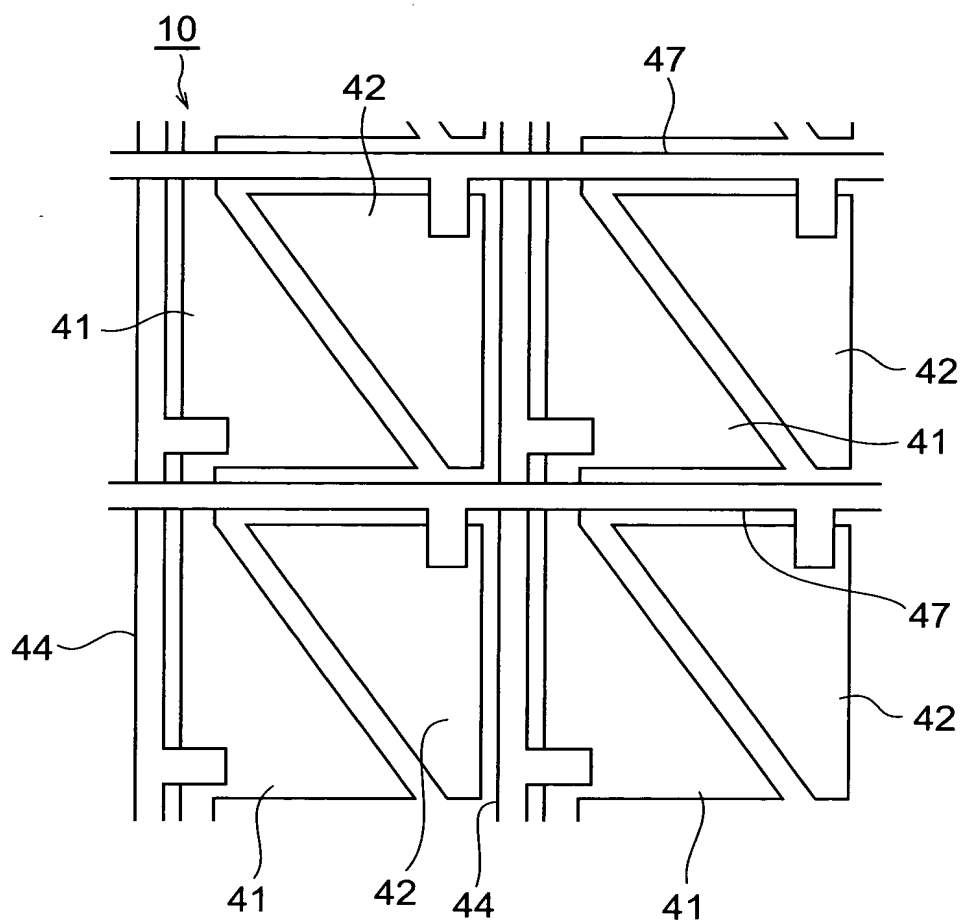
**Fig.1**

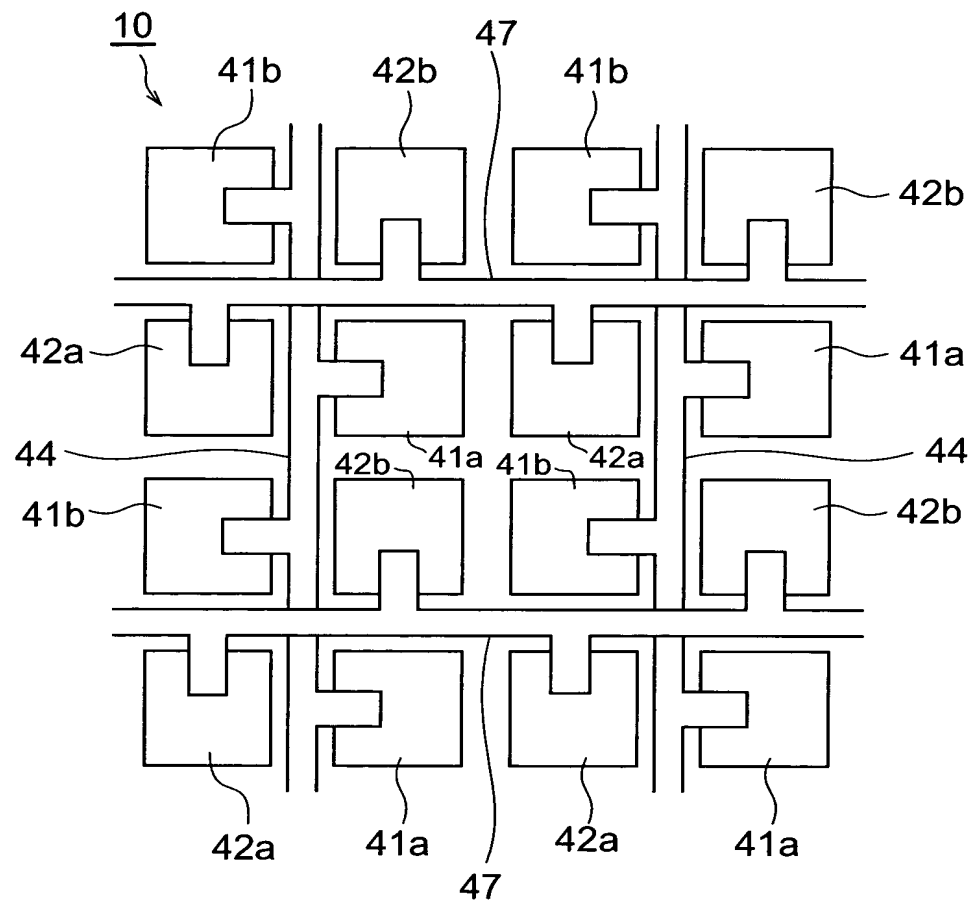
**Fig.2**



**Fig.4**

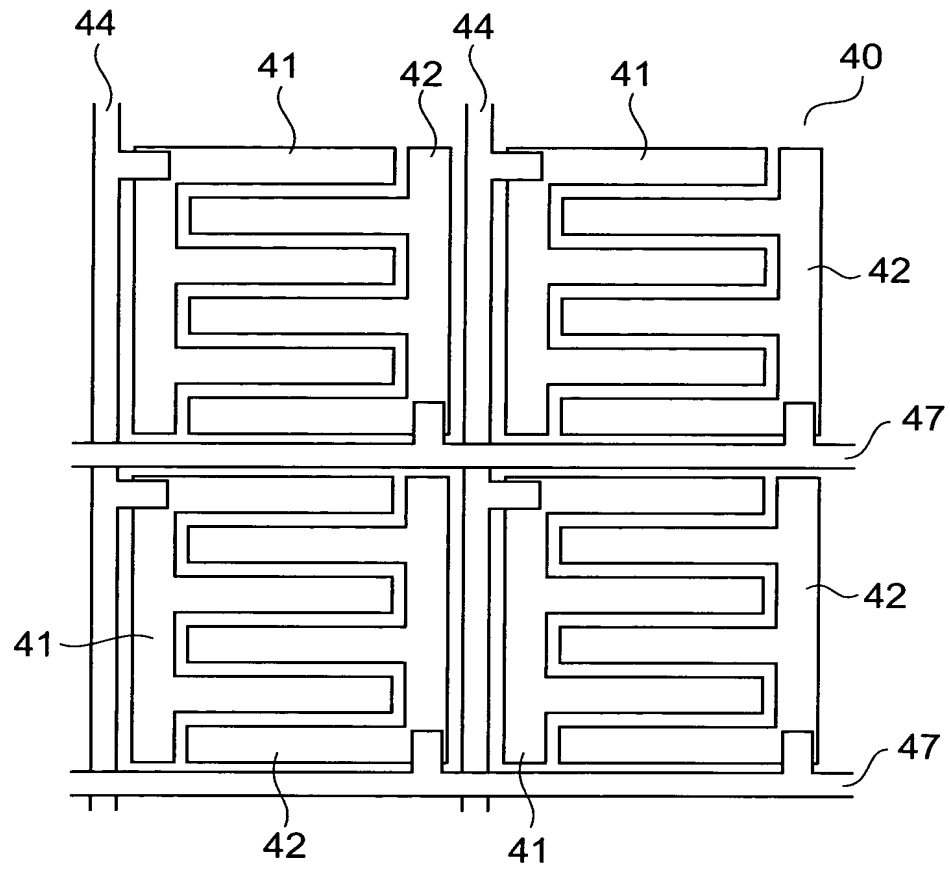


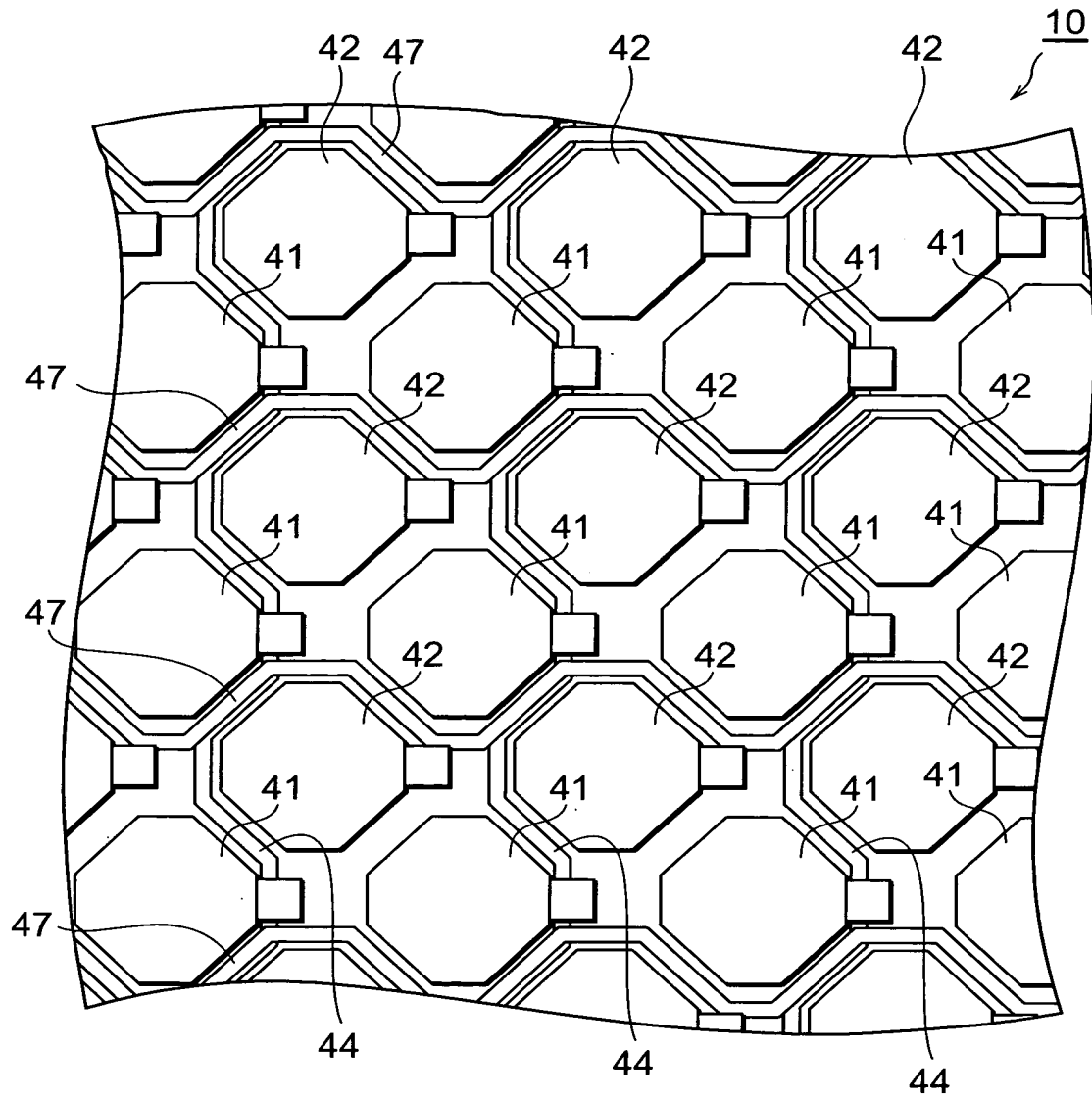
**Fig.5**

**Fig.6**

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**Fig.7**

**Fig.8**



**Fig.9**

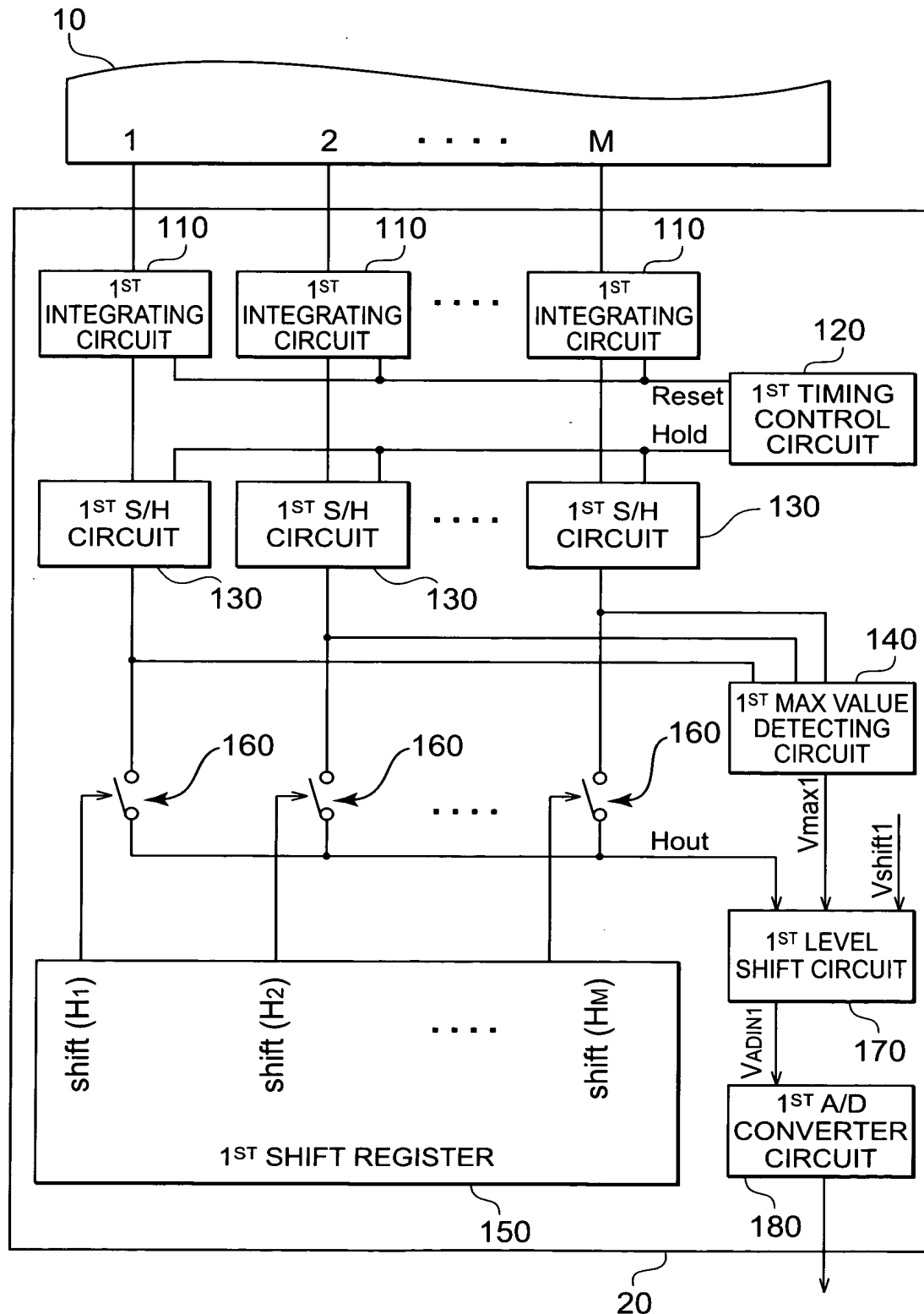
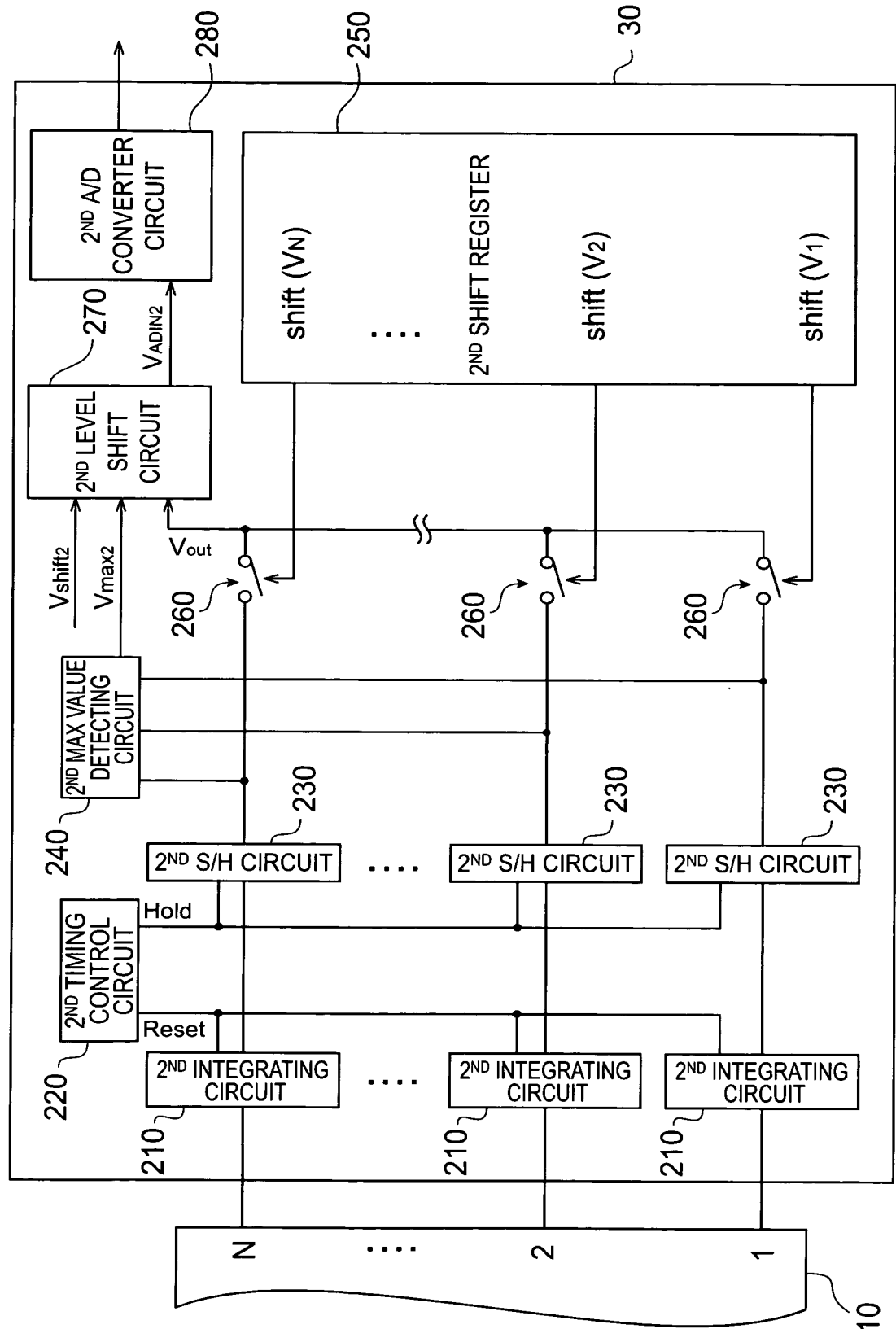
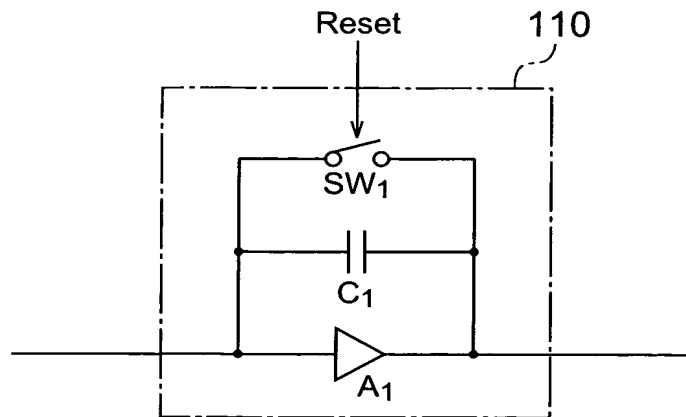
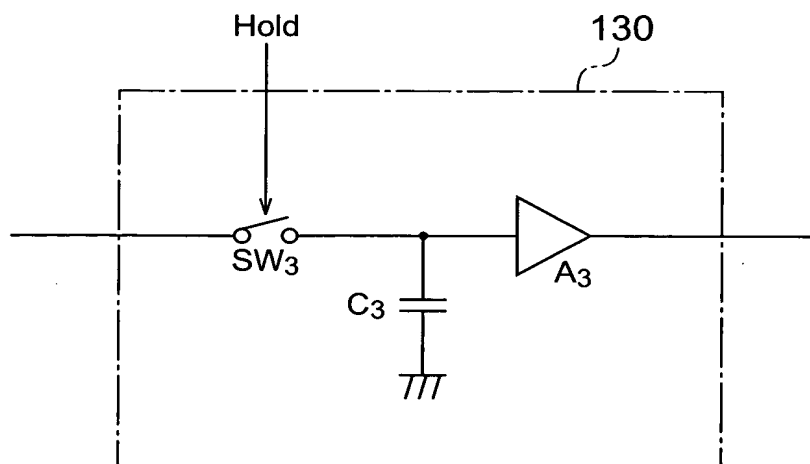


Fig. 10



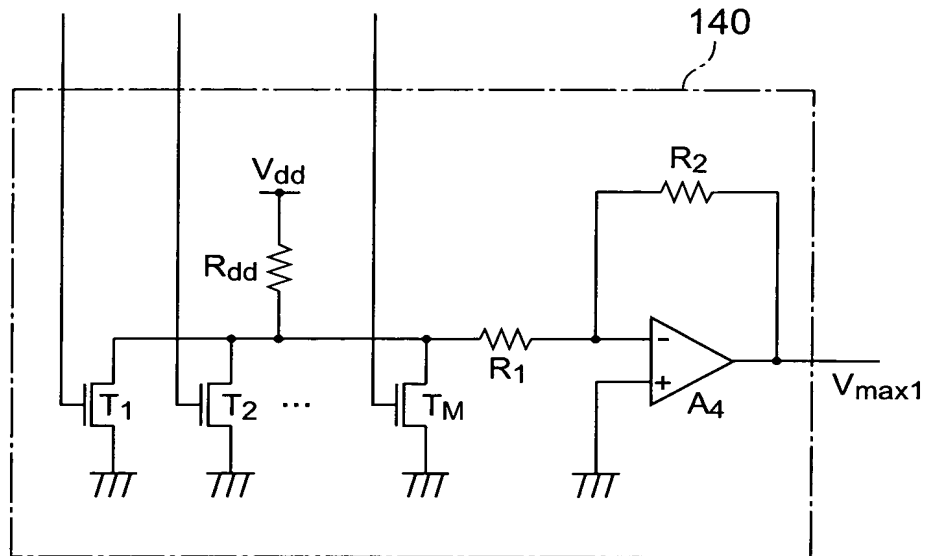
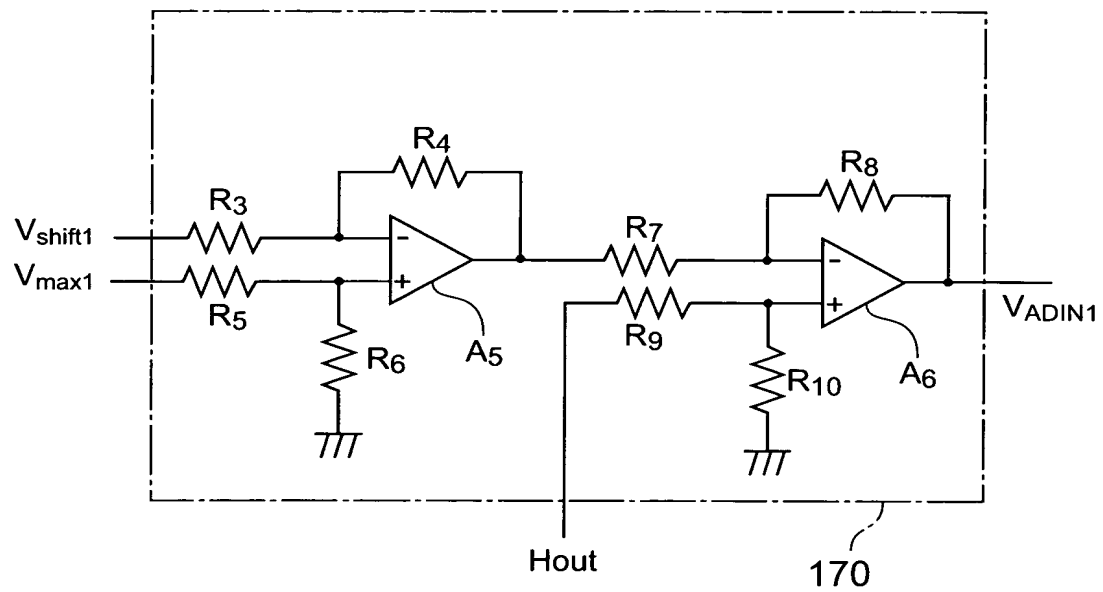
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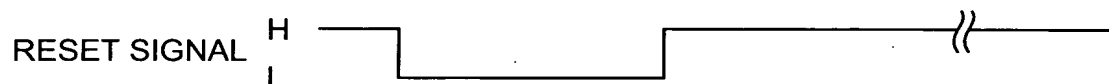
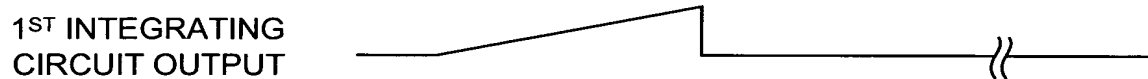
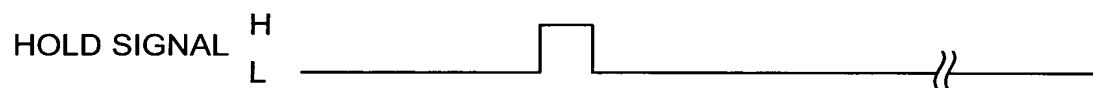
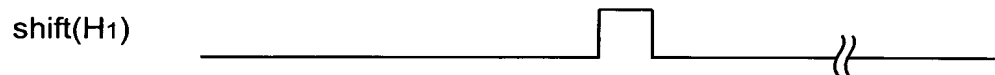
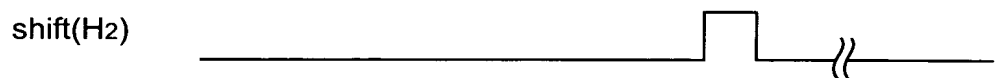
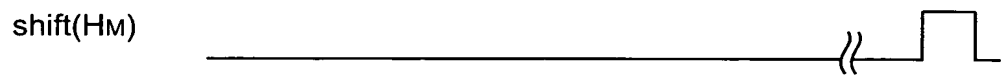
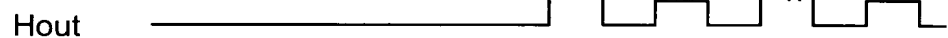
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**Fig.11****Fig.12**

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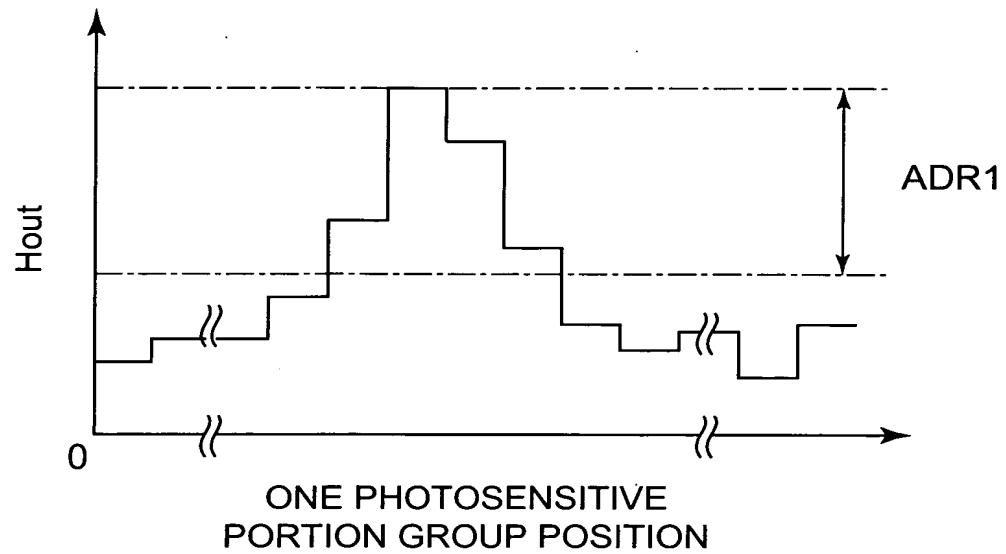
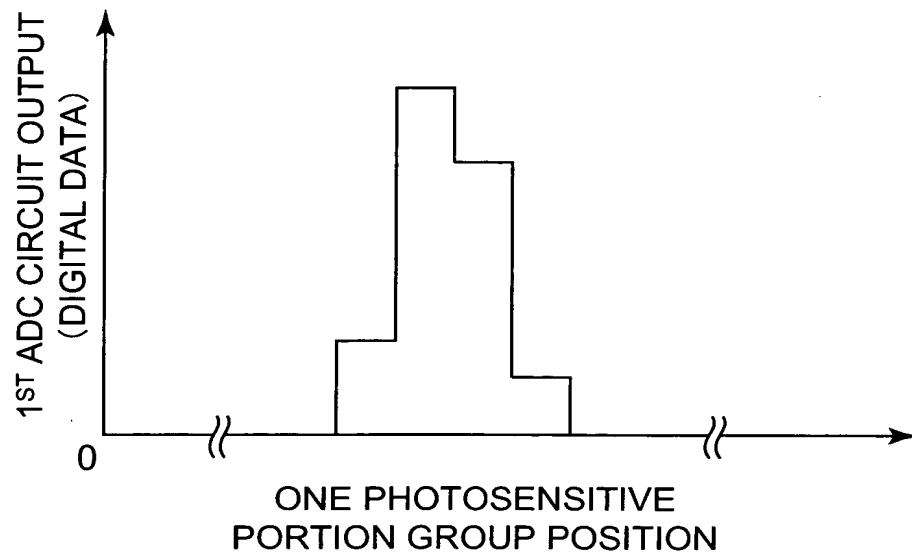
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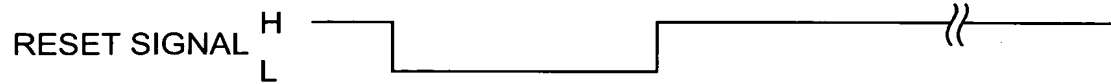
**Fig.13****Fig.14**

**Fig.15A****Fig.15B****Fig.15C****Fig.15D****Fig.15E****Fig.15F****Fig.15G****Fig.15H**

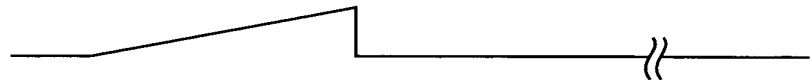
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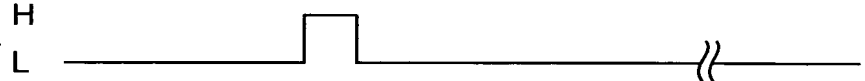
**Fig.16****Fig.17**

**Fig.18A****Fig.18B**

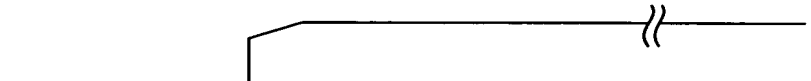
2<sup>ND</sup> INTEGRATING  
CIRCUIT OUTPUT

**Fig.18C**

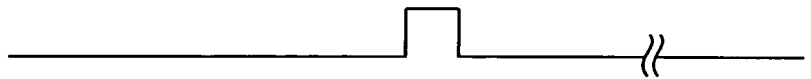
HOLD SIGNAL

**Fig.18D**

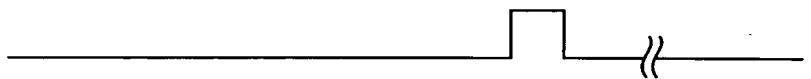
2<sup>ND</sup> S/H  
CIRCUIT OUTPUT

**Fig.18E**

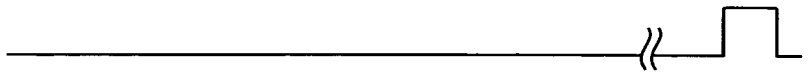
shift(V1)

**Fig.18F**

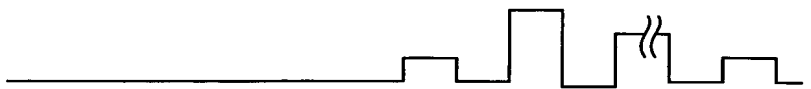
shift(V2)

**Fig.18G**

shift(VN)

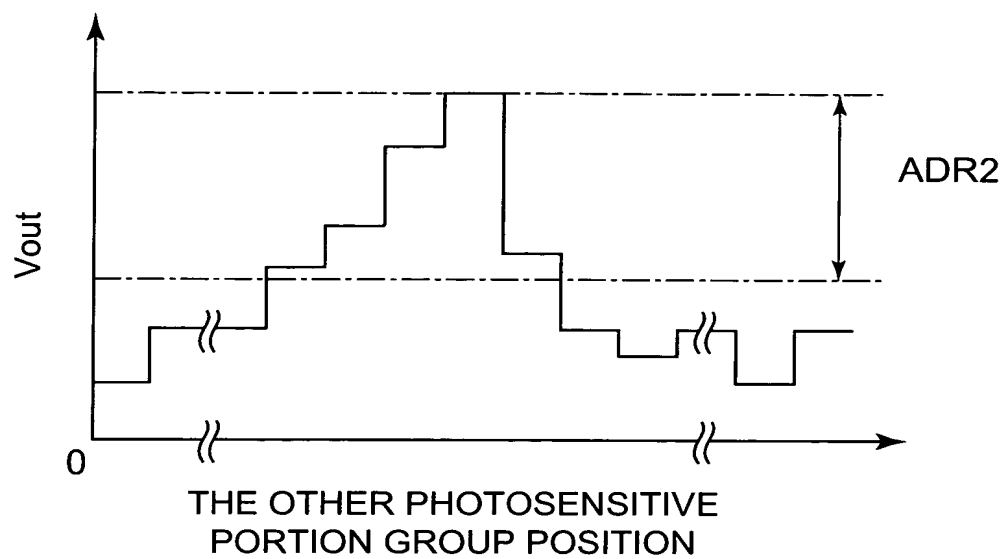
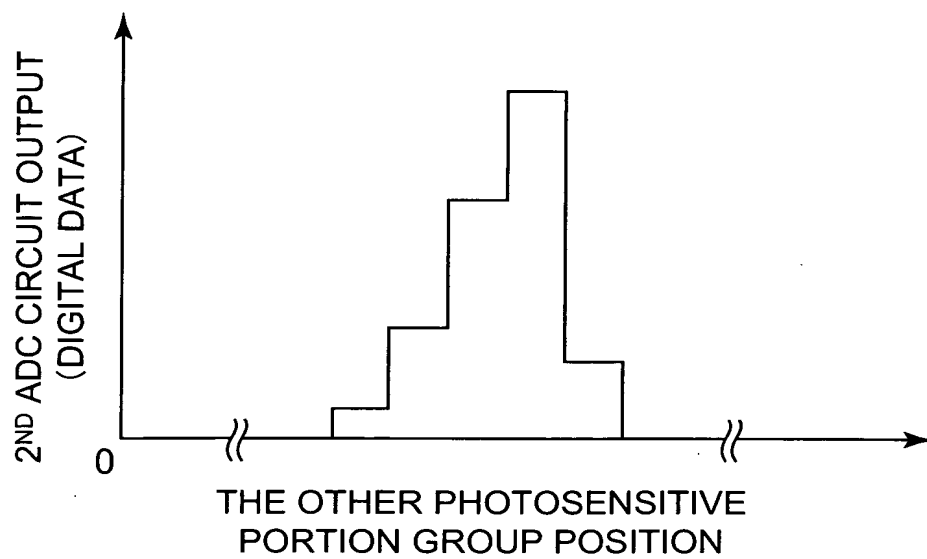
**Fig.18H**

Vout



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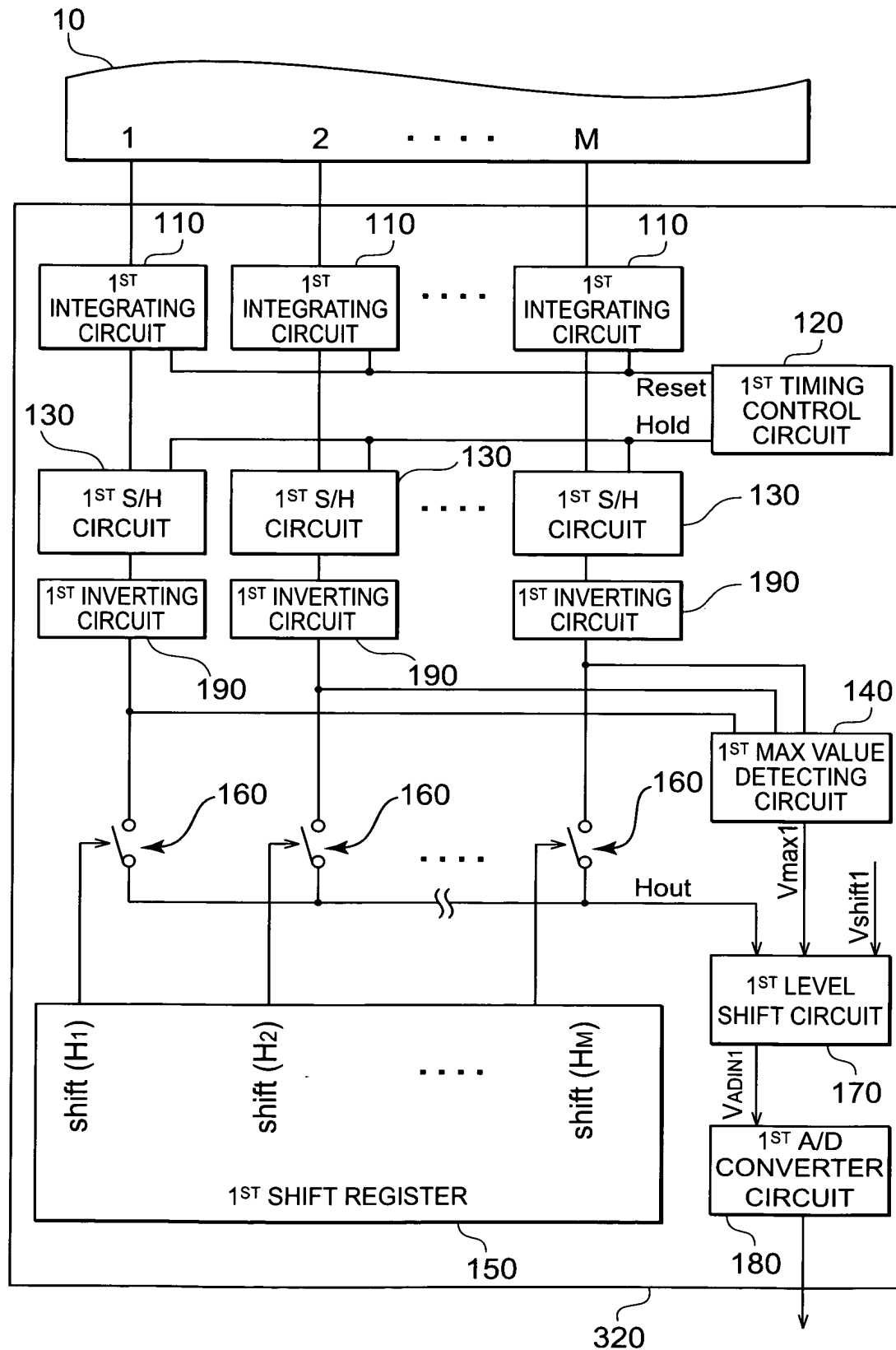
**Fig.19****Fig.20**

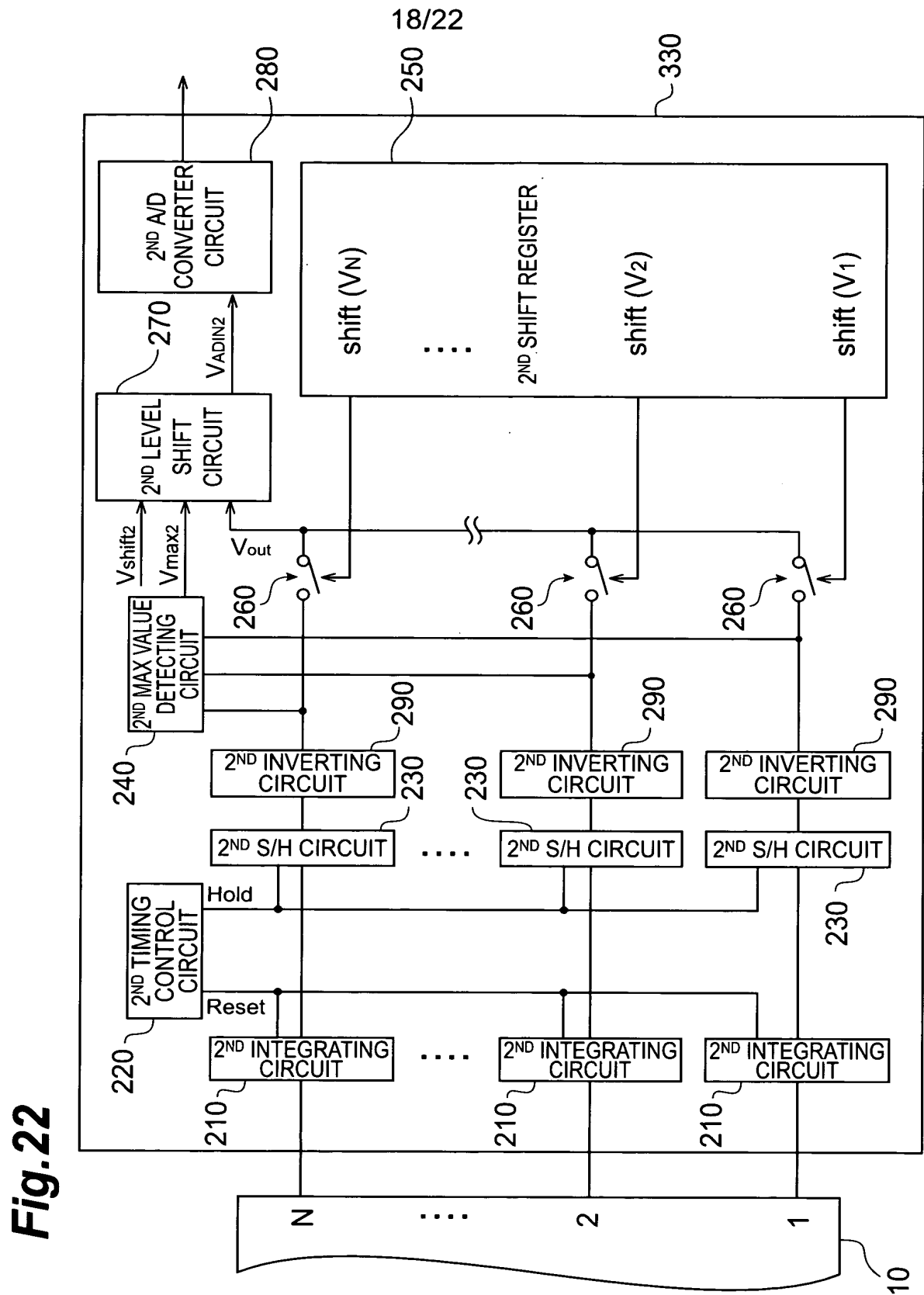


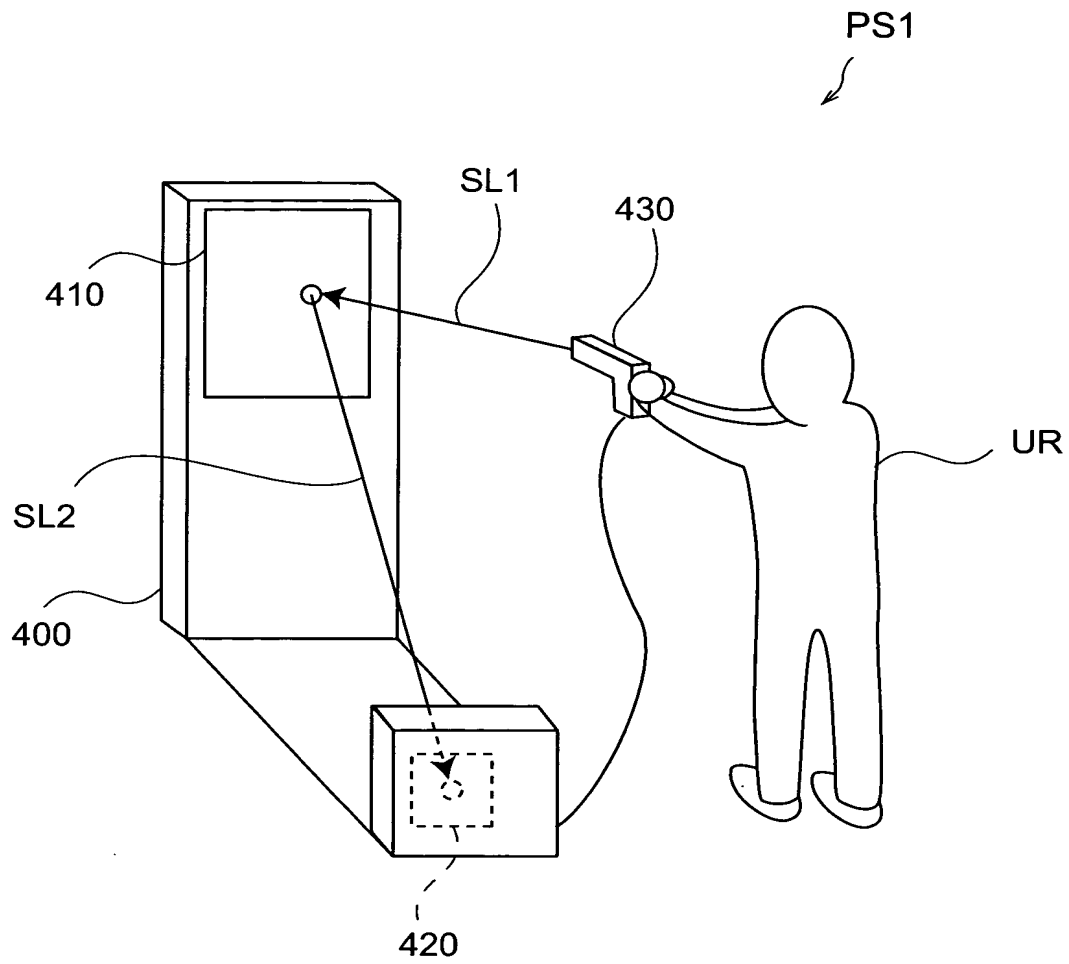
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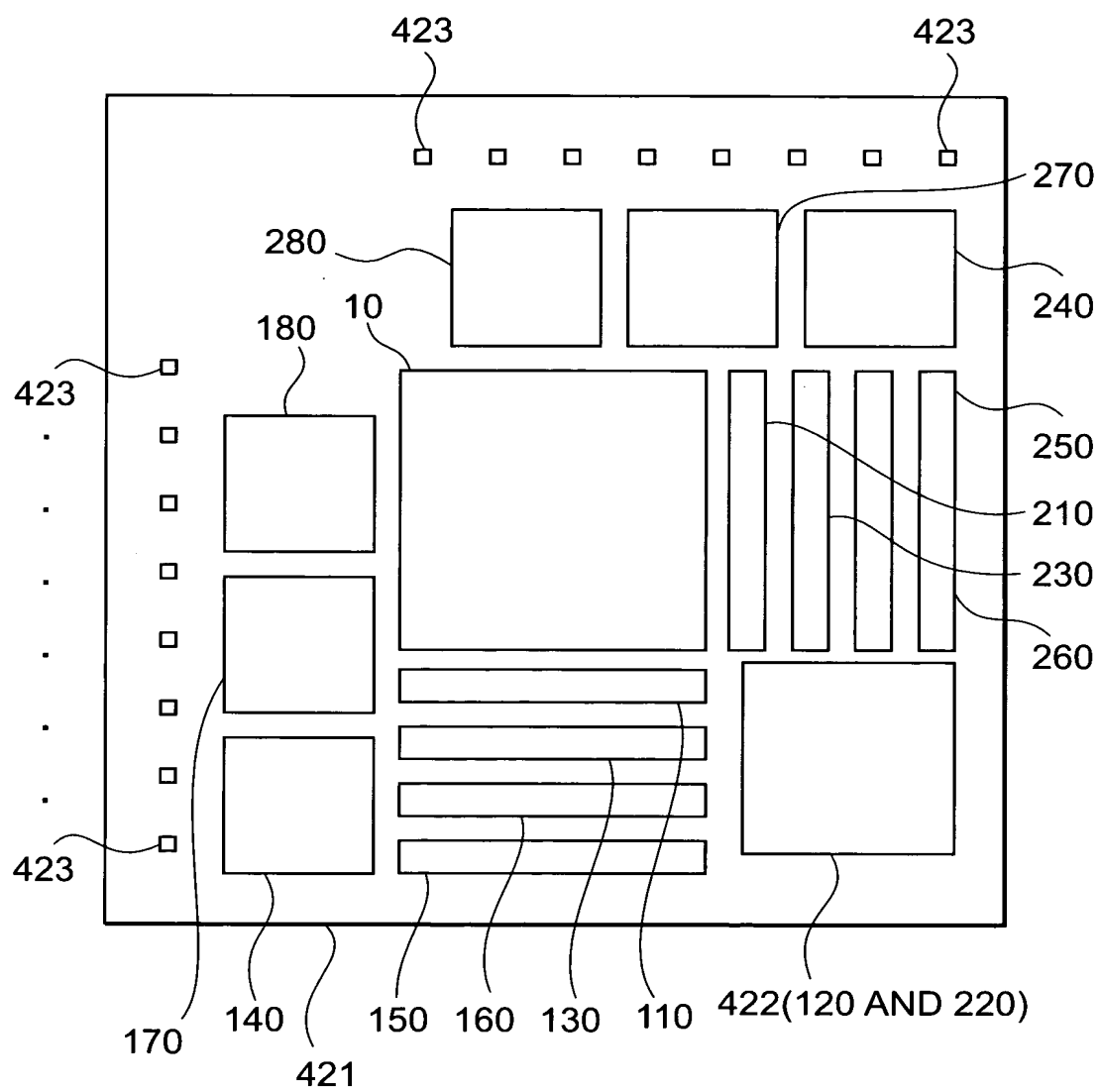
**Fig. 21**

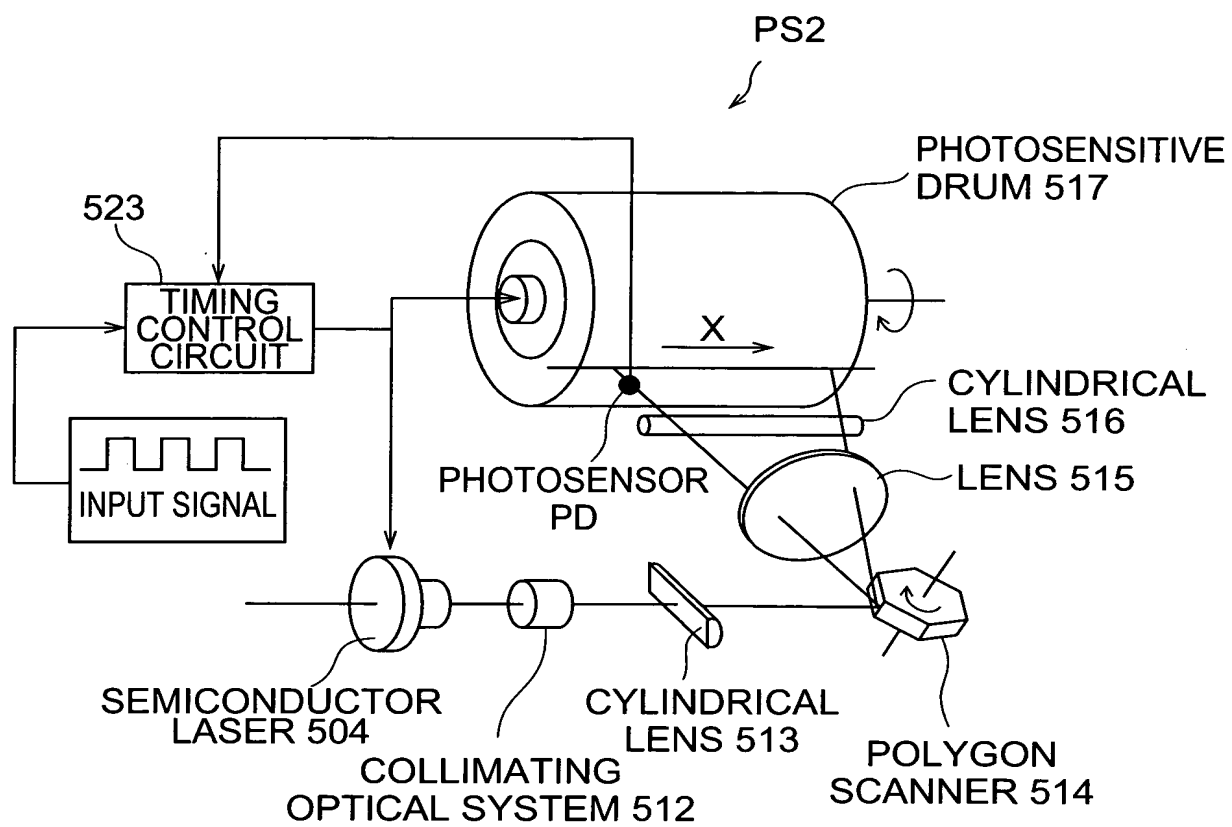
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**Fig.23**

**Fig.24**

**Fig.25**

**Fig.26**